

2 12. A printed circuit board for interconnecting an integrated circuit chip, which
comprises:

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a laminate comprising:

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8 a first layer, wherein the first layer comprises an electrically conducting
area and multiple open areas, wherein an outer perimeter of the printed
circuit board defines the axes of a Cartesian coordinate system, and
10 wherein the open areas are interspersed inside an outer perimeter of the
electrically conducting area;

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a second layer, wherein the second layer is electrically insulating, wherein
14 the second layer overlays the first layer; and

16 a third layer, wherein the third layer comprises multiple electrically
conducting traces, wherein the third layer overlays the second layer,
18 wherein at least one of the traces is oriented at other than an orthogonal
angle to each axis of the coordinate system, wherein the oriented trace is
20 longer than the spatial extension between two of the open areas, and
wherein the projection of the oriented conducting trace onto the first layer
22 lies external to the open areas.

13. The printed circuit board as recited in claim 12, wherein the open areas on the
2 first layer sum to a total open area of at least 10 percent and less than 30 percent
of the total area of the first layer.

14. The printed circuit board as recited in claim 12, further comprising:
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the integrated circuit attached to the printed circuit board.

15. The printed circuit board as recited in claim 12, further comprising:
2 a substrate attached to the laminate.
16. The printed circuit board as recited in claim 12, wherein the printed circuit board
2 is mounted in an integrated circuit package.
17. The printed circuit board as recited in claim 12, wherein the second layer material
2 is selected from the group consisting of epoxy resin and teflon.
18. The printed circuit board as recited in claim 12, further comprising:
2 a fourth layer, wherein the fourth layer is electrically insulating, wherein the first
4 layer overlays the fourth layer; and
6 a fifth layer, wherein the fifth layer comprises at least one electrically conducting
trace, wherein the fourth layer overlays the fifth layer, wherein at least one of the
8 traces is oriented at other than an orthogonal angle to each axis of the coordinate
system, wherein the oriented trace is longer than the spatial extension between
10 two of the open areas, and wherein the projection of the oriented conducting trace
onto the first layer lies external to the open areas.
19. The printed circuit board as recited in claim 18, wherein the second layer and the
2 fourth layer materials are selected from the group consisting of epoxy resin and
teflon.
20. The printed circuit board as recited in claim 12, wherein the open areas have a
2 repeating shape and a repeating size.
21. The printed circuit board as recited in claim 20, wherein the open areas have a
2 repeating orientation with respect to a Cartesian coordinate system.